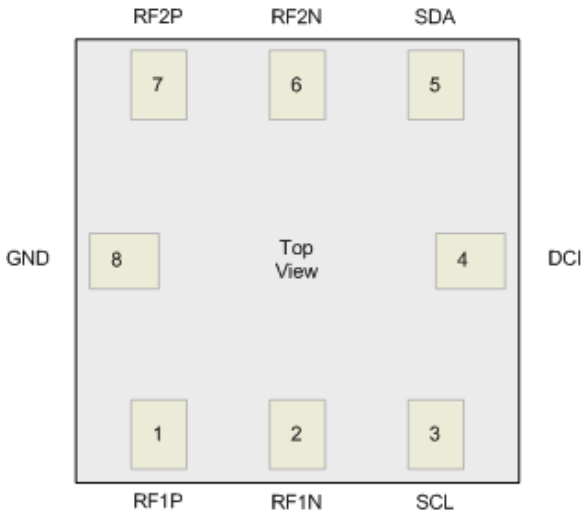
Part Order #: IPJ-P6005-X2AT

Impinj® Monza® X-8K Dura Datasheet

Rev 1.1 September 10, 2013

Monza® X-8K Dura is a UHF Gen2 RFID IC product with 8192 bits of user Non Volatile Memory (NVM) and an I2C interface.

As an I2C device Monza® X-8K Dura operates as a standard I2C EEPROM. The contents of this EEPROM can also be accessed wirelessly via the UHF Gen2 RFID Protocol.



Name	Description	Characteristic
RF1_P	Differential RF Input Port 1	1.6kΩ, 1pF –17 dBm single-port sensitivity; –19.5 dBm True3D sensitivity
RF1_N		
RF2_P	Differential RF Input Port 2	
RF2_N		
DCI	DC Input	1.6–3.6V
SCL	I2C Clock Input	VIH/L=70% / 30% DCI IOL=6mA @ 0.4V
SDA	I2C Data Input	
GND		

Features

- EPCglobal UHF Gen2 RFID air interface
- 8192 bits of user NVM
- 16 One Time Programmable (OTP) blocks (3583 bits) via blockpermalock feature supported by both I2C and EPC Gen2 interface
- QT for read control and data privacy on RF link
- I2C slave interface with NVM read and write
- –17dBm typical read sensitivity when using a single RF antenna port, -24dBm with DC input
- –19.5dBm typical read sensitivity when using dual RF antenna ports
- –12dBm typical write sensitivity when using a single RF antenna port
- I2C control of RF access
- Write wakeup mode

Table of Contents

1 Introduction

1.1 Scope

This datasheet defines the physical and logical specifications for Gen 2-compliant Monza X-8K Dura tag chip, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (Gen 2 Specification). The conventions used in the Gen 2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza X-8K Dura Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen 2 Specification.

EPC™ Tag Data Standards Specification

EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006. (Monza X-8K Dura tag chips are compliant with this Gen 2 interoperability standard.)

I2C Specification Rev. 03, June 19 2007, NXP Doc UM10204

2 Functional Description

Monza® X-8K Dura chips enable users to communicate wirelessly with the processor inside electronic devices using standard Gen 2 RFID readers, unlocking many new benefits for consumer electronics manufacturers, retailers and end users. Monza X-8K Dura connects to the processor of an electronic device through a standard I2C bus. This enables the processor to read and write the Monza X chip memory with information that is accessible to UHF Gen 2 RFID readers even when the electronic device is powered off. By enabling electronic devices to communicate with RFID readers, Monza X chips deliver a wide range of extended capabilities such as theft deterrence in the supply chain and device configuration/upgrades at point of sale and beyond.

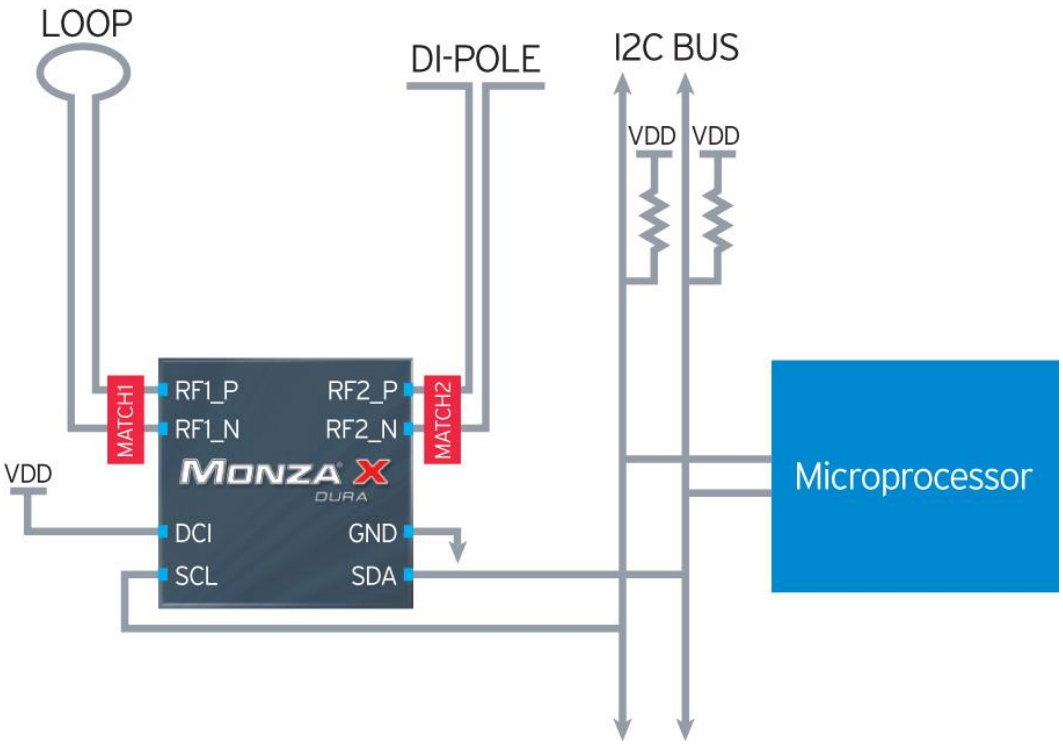
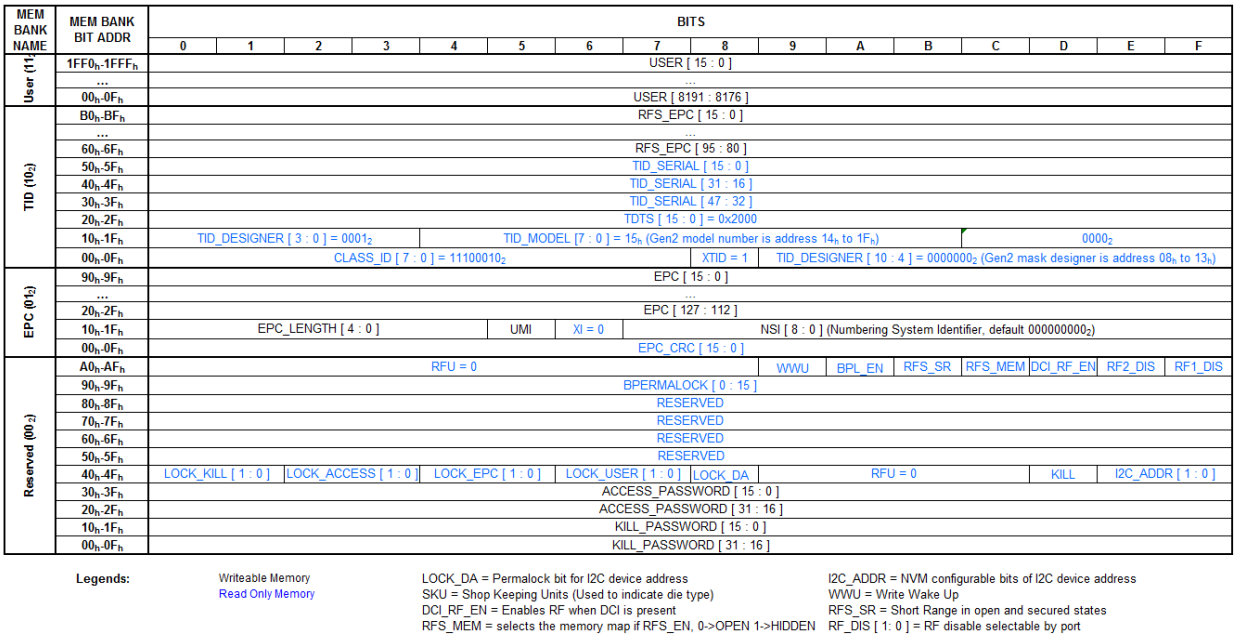


Figure 1 – Monza X-8K Dura connects with microprocessor through I2C bus

2.1 Reader Communications (Gen2/RF Commands)

A reader communicates with Monza® X-8K Dura using standard Gen2 RFID commands. Please see the EPCglobal Class-1 Generation-2 UHF RFID Air-Interface Protocol V1.2.0 for details.

The Gen 2 memory map is shown in Figure 2. Fields in blue text are read only from a Gen2 reader. Reserved memory bank words 4-10 are read only.



MEM BANK NAME	MEM BANK BIT ADDR	BITS															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
User (11_2)	$1FF0_h$-$1FFF_h$	USER [15 : 0]															
	...	...															
	00_h-$0F_h$	USER [8191 : 8176]															
TID (10_2)	$B0_h$-BF_h	RFS_EPC [15 : 0]															
	...	...															
	60_h-$6F_h$	RFS_EPC [95 : 80]															
	50_h-$5F_h$	TID_SERIAL [15 : 0]															
	40_h-$4F_h$	TID_SERIAL [31 : 16]															
	30_h-$3F_h$	TID_SERIAL [47 : 32]															
	20_h-$2F_h$	TDTS [15 : 0] = 0x2000															
	10_h-$1F_h$	TID_DESIGNER [3 : 0] = 0001_2				TID_MODEL [7 : 0] = 15_h (Gen2 model number is address 14_h to $1F_h$)								0000_2			
	00_h-$0F_h$	CLASS_ID [7 : 0] = 11100010_2								XTID = 1	TID_DESIGNER [10 : 4] = 0000000_2 (Gen2 mask designer is address 08_h to 13_h)						
EPC (01_2)	90_h-$9F_h$	EPC [15 : 0]															
	...	...															
	20_h-$2F_h$	EPC [127 : 112]															
	10_h-$1F_h$	EPC_LENGTH [4 : 0]					UMI	XI = 0	NSI [8 : 0] (Numbering System Identifier, default 000000000_2)								
	00_h-$0F_h$	EPC_CRC [15 : 0]															
Reserved (00_2)	$A0_h$-AF_h	RFU = 0									WWU	BPL_EN	RFS_SR	RFS_MEM	DCI_RF_EN	RF2_DIS	RF1_DIS
	90_h-$9F_h$	BPERMALOCK [0 : 15]															
	80_h-$8F_h$	RESERVED															
	70_h-$7F_h$	RESERVED															
	60_h-$6F_h$	RESERVED															
	50_h-$5F_h$	RESERVED															
	40_h-$4F_h$	LOCK_KILL [1 : 0]		LOCK_ACCESS [1 : 0]		LOCK_EPC [1 : 0]		LOCK_USER [1 : 0]		LOCK_DA	RFU = 0				KILL	I2C_ADDR [1 : 0]	
	30_h-$3F_h$	ACCESS_PASSWORD [15 : 0]															
	20_h-$2F_h$	ACCESS_PASSWORD [31 : 16]															
	10_h-$1F_h$	KILL_PASSWORD [15 : 0]															
	00_h-$0F_h$	KILL_PASSWORD [31 : 16]															

Legends:

Writeable Memory
Read Only Memory

LOCK_DA = Permalock bit for I2C device address
SKU = Shop Keeping Units (Used to indicate die type)
DCI_RF_EN = Enables RF when DCI is present
RFS_MEM = selects the memory map if RFS_EN, 0->OPEN 1->HIDDEN

I2C_ADDR = NVM configurable bits of I2C device address
WWU = Write Wake Up
RFS_SR = Short Range in open and secured states
RF_DIS [1: 0] = RF disable selectable by port

Figure 2– Gen2 Interface Memory Map

2.2 Support for Optional Gen 2 Commands

Following optional Gen 2 commands are supported:

Command	Code	Length	Details
Access	11000110	56	
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (000000002) if it receives a valid two-word command with an odd value pointer • Returns error code (000000002) if it receives a command for more than two words • Does not respond to block write commands of zero words
BlockPermalock	11001001	>66	• Sixteen blocks Four, 512 bits in size Twelve 128 bits in size Command can be disabled through I2C

2.3 I2C Interface (SDA, SCL, DCI Pins)

I2C is a standard two-wire interface (clock and data) that supports multiple addressable chips on a bus. Monza® X-8K Dura only supports slave capability. Monza® X-8K Dura's I2C features are compatible with the industry-standard I2C bus. Specifically Monza® X-8K Dura is compatible with I2C specification (I2C Rev 0.03, June 19 2007, NXP Doc UM10204). Monza® X-8K Dura implements the following I2C capabilities:

- I2C slave
- I2C Start Condition
- I2C Repeated Start Condition
- I2C Stop Condition
- I2C Acknowledge
- I2C 7-bit slave address with two NVM programmable bits (1101XX0)
- Fast mode transfer rates of 0-400kbits/second
- The DCI voltage provides I2C bus VOH/VOL reference and power.

When an I2C master addresses Monza® X-8K Dura it must format its write transactions as described here. In addition to the I2C device address Monza® X-8K Dura has a 16 bit, two byte, memory address that a master writes on every write transaction. The memory address specifies which memory byte the master is addressing. Only the lower 11 bits of the memory address are used. The master should set the upper bits of the memory address A15-A11 to zero.

The memory address stored in Monza® X-8K Dura is only updated explcitly during a write transaction (R/W == 0). A master only writes a memory address, and future read transactions use the previously written address. A diagram of a transaction that writes the memory address is shown in Figure 3. All bit positions are explicitly shown so the boundary between the I2C device address and the Monza® X-8K Dura memory address is clear. Subsequent diagrams do not explicitly show these address bits.

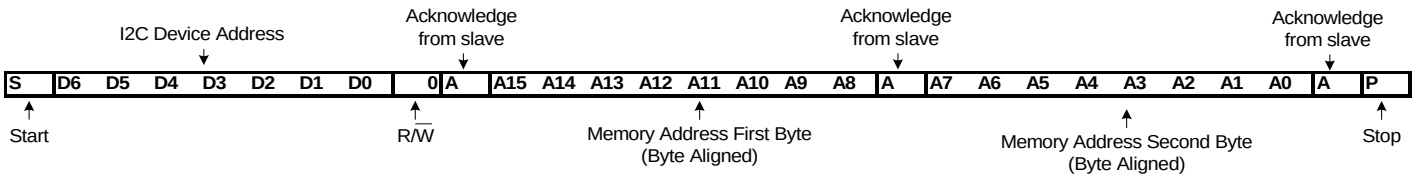


Figure 3 – Addressing the device and setting the memory address

When performing an NVM write a master transmits data after the memory address. Monza® X-8K Dura's NVM is organized as 16-bit words. Writes must align on word boundaries. The NVM allows one- or two-word writes (equivalent to two- or four-byte writes). When executing a one-word write Monza® X-8K Dura ignores the LSB (A0) of the memory address. When executing a two-word write Monza® X-8K Dura ignores the two LSBs (A1, A0) of the memory address. If the write transaction is valid then Monza® X-8K Dura begins the NVM write after receiving a stop from the I2C master. Monza® X-8K Dura will not respond to subsequent I2C transactions for the duration of the NVM write operation. The write time for one- and two-word write operations is the same. A one-word NVM write transaction is shown in Figure 4.

Monza® X-8K Dura may observe several types of invalid NVM-write transactions. If a master sends one or three data bytes then Monza® X-8K Dura will not perform the write (recall that Monza® X-8K Dura writes 16-bit words). If a master sends more than two words then Monza® X-8K Dura will not perform the write. Monza® X-8K Dura also checks the memory address and will not perform a write if the address is invalid (but note that Monza® X-8K Dura updates its memory address even if the address is invalid).

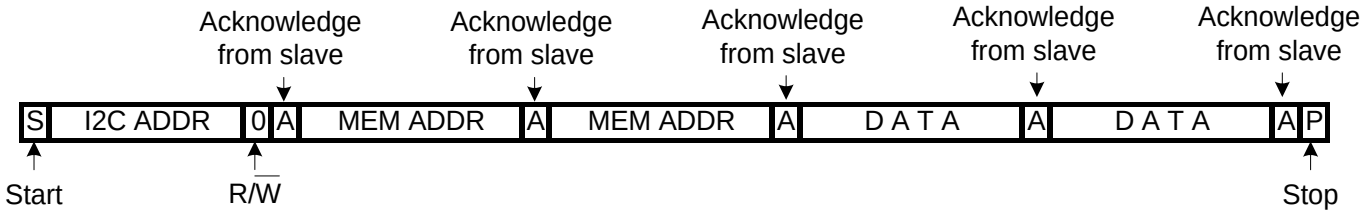


Figure 4 – One-word Monza® X-8K Dura write transaction

Figure 5 shows a read transaction. The read starts from the stored address. Monza® X-8K Dura increments the address as it sends each data byte.

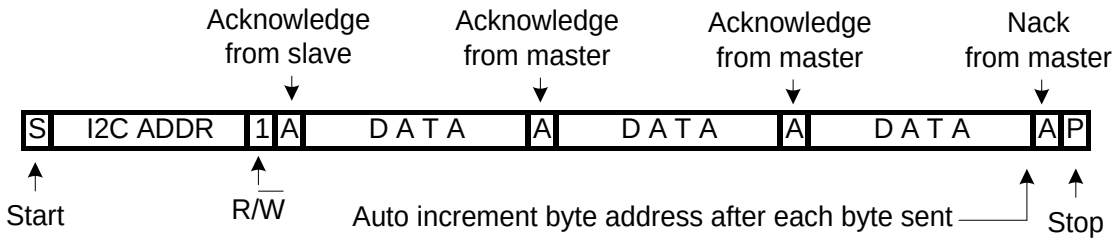


Figure 5 – Monza® X-8K Dura read transaction

Reads start from the stored address and continue to the end of memory, at which point Monza® X-8K Dura will cease exchanging data over I2C. Monza® X-8K Dura will send all ones if the master continues to read beyond the end of the memory. To read from a new location the master must send a new address. The master may halt the read at a byte boundary and later initiate a new read transaction starting from that byte. For completeness the combined write transaction then read transaction is shown in Figure 6.

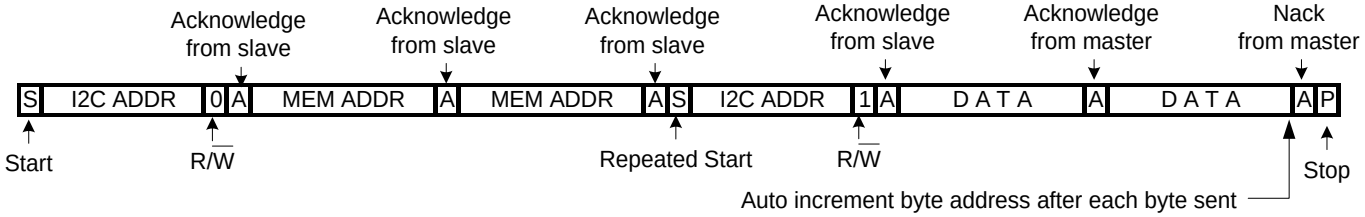


Figure 6 – Write transaction to set address followed by repeated start and read transaction.

Monza® X-8K Dura ignores all Gen2 Lock, Kill permissions when reading / writing over I2C. The I2C port has read access to the entire NVM. The I2C port has write access to most, but not all, of the NVM. Monza® X-8K Dura precludes a master from writing its manufacturing calibration fields (shown as Reserved in the I2C memory map of Figure 7); these locations are read-only.

2.4 I2C Memory Map

Gen 2 and I2C have different views on how a memory map is organized. In I2C everything is done according to bytes. One uses byte addressing, byte writing, and byte reading. In Gen2 things are done in terms of bits or 16 bit words.

Monza® X-8K Dura is a hybrid of these two approaches. It forces I2C to do one word or two word writes, but allows for byte wise reading and addressing. When reading via I2C the first bit read is always bit seven within the byte. The next byte read is at the next higher I2C byte address. The I2C memory map in byte wise format is shown in Figure 7.

An additional memory map that shows bit addressing from I2C in a word wise format is shown in Figure 8.

GEN2 BANK NAME	I2C BYTE ADDR	BIT ADDRESS in BYTE								I2C Perm
		7	6	5	4	3	2	1	0	
USER (11_2)	1087	USER								R/W
	1086	USER								R/W
	. . .	USER								R/W
	66	USER								R/W
	64	USER								R/W
	63	QT_EPC								R/W
	62	QT_EPC								R/W
	. . .	QT_EPC								R/W
	52	QT_EPC								R/W
TID (10_2)	51	TID_SERIAL (Byte 5)								R
	50	TID_SERIAL (Byte 4)								R
	49	TID_SERIAL (Byte 3)								R
	48	TID_SERIAL (Byte 2)								R
	47	TID_SERIAL (Byte 1)								R
	46	TID_SERIAL (Byte 0)								R
	45	0x00								R
	44	0x20								R
	43	TID_MODEL [7 : 0] =01010000_2								R
	42	TID_DESIGNER [3 : 0] = 0001_2				TID_MODEL [11 : 8] = 0001_2				R
	41	XTID = 1	TID_DESIGNER [10 : 4] = 0000000_2 (Gen2 mask designer is address 08_h to 13_h)							R
	40	CLASS_ID [7 : 0] = 11100010_2								R
EPC (01_2)	39	EPC								R/W
	38	EPC								R/W
	. . .	EPC								R/W
	24	EPC								R/W
	23	NSI [7 : 0]								R/W
	22	EPC_LENGTH [4 : 0]					UMI	XI (NVM)	NSI [8]	R/W
Reserved (00_2)	21	RFU = 0	WWU	BPL_EN	QT_SR	QT_MEM	DCI_RF_EN	RF2_DIS	RF1_DIS	R/W
	20	RFU (WRITE as 00000000_2)								R/W
	19	BLOCK_PERMALOCK [8 : 15]								R/W
	18	BLOCK_PERMALOCK [0 : 7]								R/W
	17	RESERVED								R
	. . .	RESERVED								R
	10	RESERVED								R
	9	LOCK_DA	RFU = 0000_2				KILL	I2C_ADDR [1 : 0]		R/W
	8	LOCK_KILL [1 : 0]	LOCK_ACCESS [1 : 0]		LOCK_EPC [1 : 0]			LOCK_USER [1 : 0]		R/W
	7	ACCESS_PASSWORD								R/W
	6	ACCESS_PASSWORD								R/W
	5	ACCESS_PASSWORD								R/W
	4	ACCESS_PASSWORD								R/W
	3	KILL_PASSWORD								R/W
	2	KILL_PASSWORD								R/W
	1	KILL_PASSWORD								R/W
	0	KILL_PASSWORD								R/W

I2C_ADDR = TWO LSBs of I2C address
DCI_RF_EN = Enables RF when DCI is present (SKU_A)
RFS_MEM = selects the memory map if RFS_EN, 0->OPEN 1->HIDDEN
LOCK_DA = Permalock bit for I2C Device Address
RFS_SR = Short Range in open and secured states
RF_DIS [1: 0] = RF disable selectable by port

Figure 7 – I2C Interface Memory Map in a Byte Wise format

GEN2 BANK NAME	I2C Bit ADDR	BIT ADDRESS 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	I2C PERM
User (11)	$21F0_h$-$21FF_h$	USER [15 : 0]																W
	...	...																W
	2000_h-$20F_h$	USER [8191 : 8176]																W
TID (10_2)	$1F0_h$-$1FF_h$	RFS_EPC [15 : 0]																W
	...	...																W
	$1A0_h$-$1AF_h$	RFS_EPC [95 : 80]																W
	190_h-$19F_h$	TID_SERIAL [15 : 0]																R
	180_h-$18F_h$	TID_SERIAL [31 : 16]																R
	170_h-$17F_h$	TID_SERIAL [47 : 32]																R
	160_h-$16F_h$	TDTS [15 : 0] = 0x2000																R
	150_h-$15F_h$	TID_DESIGNER [3 : 0] = 0001_2				TID_MODEL [7 : 0] = 15_h (Gen2 model number is address 14_h to $1F_h$)								0000_2				R
	140_h-$14F_h$	CLASS_ID [7 : 0] = 11100010_2								XTID = 1	TID_DESIGNER [10 : 4] = 0000000_2 (Gen2 mask designer is address 08_h to 13_h)							R
EPC (01_2)	130_h-$13F_h$	EPC [15 : 0]																W
	...	...																W
	$C0_h$-CF_h	EPC [127 : 112]																W
	$B0_h$-BF_h	EPC_LENGTH [4 : 0]					UMI	XI = 0	NSI [8 : 0] (Numbering System Identifier, default 000000000_2)									W
Reserved (00_2)	$A0_h$-AF_h	RFU = 0									WWU	BPL_EN	RFS_SR	RFS_MEM	DCI_RF_EN	RF2_DIS	RF1_DIS	W
	90_h-$9F_h$	BPERMALOCK [0 : 15]																W*
	80_h-$8F_h$	RESERVED																R
	70_h-$7F_h$	RESERVED																R
	60_h-$6F_h$	RESERVED																R
	50_h-$5F_h$	RESERVED																R
	40_h-$4F_h$	LOCK_KILL [1 : 0]		LOCK_ACCESS [1 : 0]		LOCK_EPC [1 : 0]		LOCK_USER [1 : 0]		LOCK_DA	RFU = 0					KILL	I2C_ADDR [1 : 0]	W
	30_h-$3F_h$	ACCESS_PASSWORD [15 : 0]																W
	20_h-$2F_h$	ACCESS_PASSWORD [31 : 16]																W
	10_h-$1F_h$	KILL_PASSWORD [15 : 0]																W
	00_h-$0F_h$	KILL_PASSWORD [31 : 16]																W

Legends: ROM, NVM

W* = Bits are writable from I2C but some are sticky. See Block Permalock implementaiton for details
BPERMALOCK[0:15] = Block Permalock bits
I2C_ADDR = NVM configurable bits of I2C device ID
DCI_RF_EN = Enables RF when DCI is present
RFS_SR = Short Range in open and secured states
RFS_MEM = selects the memory map if RFS_EN, 0->OPEN 1->HIDDEN
RF_DIS [1: 0] = RF disable selectable by port

Figure 8 – I2C Interface Memory Map in a Word Wise format

2.5 I2C Control of Monza® X-8K Dura Behavior

The I2C interface can control Monza® X-8K Dura behavior by writing to bytes 8 or 9, 18 or 19, 20 or 21 and 22 or 23. The following sections describe how control bits in these words change the behavior.

2.6 Monza® X-8K Dura I2C and Gen2 Lock Bits

The lock bits for the kill password (LOCK_KILL[1:0]), the access password LOCK_ACCESS[1:0]), the EPC memory bank (LOCK_EPC[1:0]), and the USER memory bank (LOCK_ USER[1:0]) are in byte eight of memory. In each of these lock bit pairs bit one corresponds to pwd-write or pwd-read/write and bit zero corresponds to the permalock bit. Note that the I2C can always change the state of these bits and that their permissions only apply to the RF Gen2 interface.

Table 2.1 – *Lock* Bit-field functionality

pwd-write	permalock	Description
0	0	Associated memory bank is writeable from either the **open** or **secured** states.
0	1	Associated memory bank is permanently writeable from either the **open** or **secured** states and may never be locked.
1	0	Associated memory bank is writeable from the **secured** state but not from the **open** state.
1	1	Associated memory bank is not writeable from any state.
pwd-read/write	**permalock**	**Description**

0	0	Associated password location is readable and writeable from either the **open** or **secured** states.
0	1	Associated password location is permanently readable and writeable from either the **open** or **secured** states and may never be locked.
1	0	Associated password location is readable and writeable from the **secured** state but not from the **open** state.
1	1	Associated password location is not readable or writeable from any state.

2.7 Monza® X-8K Dura I2C and Gen2 BlockPermalock

Monza® X-8K Dura will segments user memory into 16 blocks. Blocks zero through 15 may be blockpermalocked from either the Gen2 interface or the I2C interface. A blockpermalocked block allows reads but not writes to the block. Blockpermalocking is permanent for blocks one through 15 and may not be unlocked from either interface. The blockpermalock may be undone for block zero from the I2C interface and I2C ignores the blockpermalock permission for block zero.

The five blocks as seen from the I2C interface are shown in Figure 9. The figure includes the Gen 2 User memory bank bit addresses of the blocks and the I2C byte addresses of the blocks. Note that a large portion of the User memory bank has no permalock blocks. Please see the Gen2 specification for details on how a reader may lock the memory via *BlockPermaLock* command.

The mechanism for a microprocessor permalocking over I2C is as follows: Execute a one-word (2 byte) write to bytes 18 and 19 (word address nine). There are sixteen blockpermalock bits in bytes 18 and 19 that control the write permission to the 16 user-memory blocks. Monza® X-8K Dura will bitwise OR each of the current permalock bits with the 15 bits corresponding to blocks one through 15 and write the updated word into NVM. Block zero may be unlocked via the I2C interface. Monza® X-8K Dura does not allow unlocking of blockpermalocked memory in blocks one through 15 via either the Gen2 interface or I2C interface.

To control the Gen2 interface access to the *BlockPermalock* command the I2C interface will have a *BlockPermalock* command enable bit that only it can write to. When the bit is set Monza® X-8K Dura will execute valid *BlockPermalock* commands and when it is cleared it will ignore all *BlockPermalock* commands. The location of the BPL_EN bit is in bit five of byte 21.

Gen2 User Memory Bank Bit Address Range	I2C Byte Address Range	BLOCKS	I2C Block Perma Lockable	Gen2 Block Perma Lockable
3584 - 8191	512 - 1087	Rest of User Memory (No BlockPermalock Blocks)	No	No
3456 - 3583	496 - 511	BLOCK 15 (128 bits)	Yes	Yes
3328 - 3455	480 - 495	BLOCK 14 (128 bits)	Yes	Yes
3200 - 3327	464 - 479	BLOCK 13 (128 bits)	Yes	Yes
3072 - 3199	448 - 463	BLOCK 12 (128 bits)	Yes	Yes
2944 - 3071	432 - 447	BLOCK 11 (128 bits)	Yes	Yes
2816 - 2943	416 - 431	BLOCK 10 (128 bits)	Yes	Yes
2688 - 2815	400 - 415	BLOCK 9 (128 bits)	Yes	Yes
2560 - 2687	384 - 399	BLOCK 8 (128 bits)	Yes	Yes
2432 - 2559	368 - 383	BLOCK 7 (128 bits)	Yes	Yes
2304 - 2431	352 - 367	BLOCK 6 (128 bits)	Yes	Yes
2176 - 2303	336 - 351	BLOCK 5 (128 bits)	Yes	Yes
2048 - 2175	320 - 335	BLOCK 4 (128 bits)	Yes	Yes
1536 - 2047	256 - 319	BLOCK 3 (512 bits)	Yes	Yes
1024 - 1535	192 - 255	BLOCK 2 (512 bits)	Yes	Yes
512 - 1023	128 - 191	BLOCK 1 (512 bits)	Yes	Yes
0 - 511	64 - 127	BLOCK 0 (512 bits)	No	Yes

Figure 9 – BlockPermaLock blocks as seen from the I2C interface

2.8 Monza® X-8K Dura I2C Control of LOCK_DA and I2C_ADDR[1:0] Bits

The I2C_ADDR[1:0] bits contain the I2C device address bits D2 and D1 respectively. These bits are meant to be reconfigurable in order to avoid address conflicts on the I2C bus. The LOCK_DA bit is a permalock bit that should be set once the I2C device address is selected. Once the LOCK_DA bit is set the value of the LOCK_DA bit and I2C_ADDR[1:0] are preserved by the chip during all writes to bytes 8 and 9.

2.9 Monza® X-8K Dura Control of the QT Function

The QT_SR and QT_MEM bits control in byte 21 control the QT functionality of Monza® X-8K Dura. They have no effect on I2C operation and only change RF Gen2 behavior. The two bits operate independently from each other. The QT_SR bit turns on Monza® X-8K Dura's short range mode when it is set. When Monza® X-8K Dura is in short range, operations in OPEN or SECURED states are required to be close to the reader. Note, however, that if the Monza® X-8K Dura antenna has a gain < -9dBi, there will be no OPEN or SECURED access through the RF port when the QT_SR bit is set. The QT_MEM bit controls how Monza® X-8K Dura's memory appears to the Gen2 interface. When the bit is set Monza® X-8K Dura is in public mode: user memory bank is hidden, TID serialization is hidden, and uses its QT_EPC in the EPC bank. When the bit is cleared Monza® X-8K Dura is in private mode and all of its memory is exposed. The memory map in Figure 2 shows the Monza® X-8K Dura memory in private mode.

The DCI_EN_RF_EN bit the RF2_DIS bit, and the RF1_DIS bit in byte 21 are covered in the section on RF access control.

2.10 Monza® X-8K Dura I2C Control of Gen2 Response to Ack Command

The length field in byte 22 may be written from I2C. The length field specifies the number of words backscattered in response to a Gen2 *Ack* command. Byte 22 also contains an NVM space for the UMI bit which may be read or written from I2C. The Gen2 UMI bit is calculated from the bitwise or of bits five through zero in byte 40, which the reader is supposed to do. The I2C master may also do this to indicate that there is data in the user memory bank for the reader to read. The XI bit is always backscattered as a zero to the Gen2 reader even though the I2C master may read the underlying NVM bit.

2.11 RF Access Control

Monza® X-8K Dura provides three levels of control over RF access as follows:

1. Setting either or both the RF2_DIS or RF1_DIS bits in byte 21 of the NVM disables RF access on the corresponding RF port. These bits are accessible only to I2C, not RF. The factory defaults are 0, enabling RF1 and RF2.
2. Setting the DCI_RF_EN bit to 0 in byte 21 of the NVM inhibits all RF access when DCI voltage is present. This takes precedence over the state of the RF1_DIS, RF2_DIS bit in #1 above. This bit is also only accessible from I2C, not RF. This bit is set by factory default to 0. Thus, by default, there is RF access to RF1, RF2 when DCI voltage is NOT present and no RF access when DCI voltage is present. The specification $\mathbf{V_{RFON}}$ determines the DCI voltage that inhibits RF.
3. Setting the KILL bit 2 in byte 9 of the NVM will inhibit all RF access. This bit can be set from RF using a Gen2 KILL command or by writing from I2C. This is the normal mechanism for a reader to disable a chip. This KILL bit takes precedence over both #1 and #2 above. I2C can re-write this bit back to 0 and thus reverse and RF KILL command. The factory default for KILL is 0.

The factories defaults are set so Monza® X-8K Dura operates like any other RFID tag when DCI voltage is not present. When DCI voltage is present the default behavior, through mechanism #2 above, is to inhibit all RF access. The KILL bit is always set to 0 at the factory by Gen2 definition. In conventional RFID chips once this bit is set to 1 a chip is dead and can never be

resurrected. Monza® X-8K Dura, having a hard wired I2C interface, allows un-doing the KILL operation from I2C.

2.12 Gen2/I2C Arbitration

If the DCI_RF_EN bit is set to one then Monza® X-8K Dura has three different operating states as shown in Figure 10. The states are "*Internal Control"*, "*I2C Control*", and "*Idle or RF Receive*". If the DCI_RF_EN bit is set to zero then Monza® X-8K Dura will not respond to RF commands when in the *Idle or RF Receive* state.

***Internal Control*:** Monza® X-8K Dura is in *Internal Control* when (1) executing an initialization sequence, (2) writing the NVM or (3) backscattering a response to an RF command. When in *Internal Control* Monza® X-8K Dura ignores I2C transactions or RF commands.

***I2C Control*:** Monza® X-8K Dura is in *I2C Control* when a master is issuing commands to Monza® X-8K Dura over the I2C bus. I2C Control starts when Monza® X-8K Dura detects a matching device ID and is not under *Internal Control*. The I2C bus master releases control of Monza® X-8K Dura either by ending a transaction with a stop bit or by issuing a subsequent start with a non-matching device ID. If Monza® X-8K Dura was commanded to perform an NVM write then it moves to *Internal Control*, otherwise it returns to idle. When in *I2C Control* Monza® X-8K Dura ignores all RF commands. Note that the master may stall the I2C bus (by holding SCL low) in the middle of a transaction and prevent RF access until releasing the bus.

***Idle or RF Receive*:** Monza® X-8K Dura is in *Idle or RF Receive* when receiving an RF command or when idle. After receiving a command Monza® X-8K Dura transitions to *Internal Control* to execute the command. Executing a command may cause Monza® X-8K Dura to (1) backscatter a reply (2) write to NVM or (3) change internal states. An I2C transaction may interrupt Monza® X-8K Dura in *Idle or RF Receive*– by this means the I2C port exercises priority over the RF port and may not be locked out. Note that I2C is locked out when Monza® X-8K Dura transitions to *Internal Control* to execute the command.

In certain operating states and under certain conditions Monza® X-8K Dura may appear unresponsive to an I2C master for up to 20 milliseconds (During a slow Gen2 backscatter). This datasheet recommends that an I2C master have a retry algorithm that can accommodate Monza® X-8K Dura being busy.

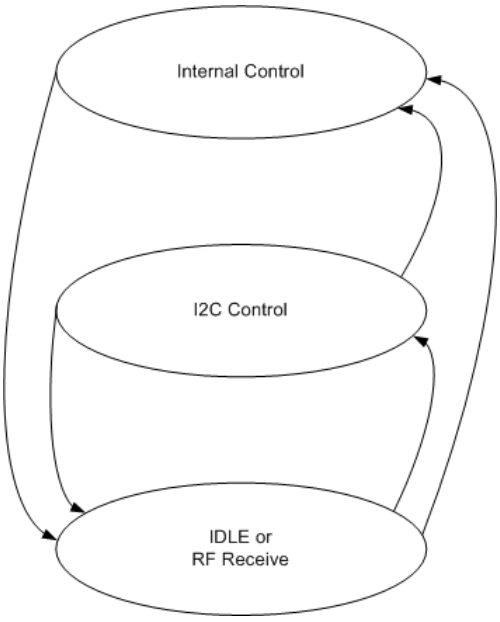


Figure 10 – Monza® X-8K Dura operating states

2.13 Write Wakeup Mode

Monza® X-8K Dura has a wake up feature that is tied to writes being performed over the Gen2 interface. In order to enable this feature the I2C master must set the WWU bit (bit 6 of byte 21) to one. Then the master must set the Monza® X-8K Dura's DCI pin to 0V (Sleep mode). The SCL and SDA lines must remain high, but will draw no current. A reader may continue to interact with Monza® X-8K Dura on the RF ports. If a reader performs a write operation, and the wake up bit is set, Monza® X-8K Dura will assert the SCL IO pulling the SCL line low for the duration of the write operation, approximately 4ms. This transition is detectable by the sleeping master and may be used to wake up the system.

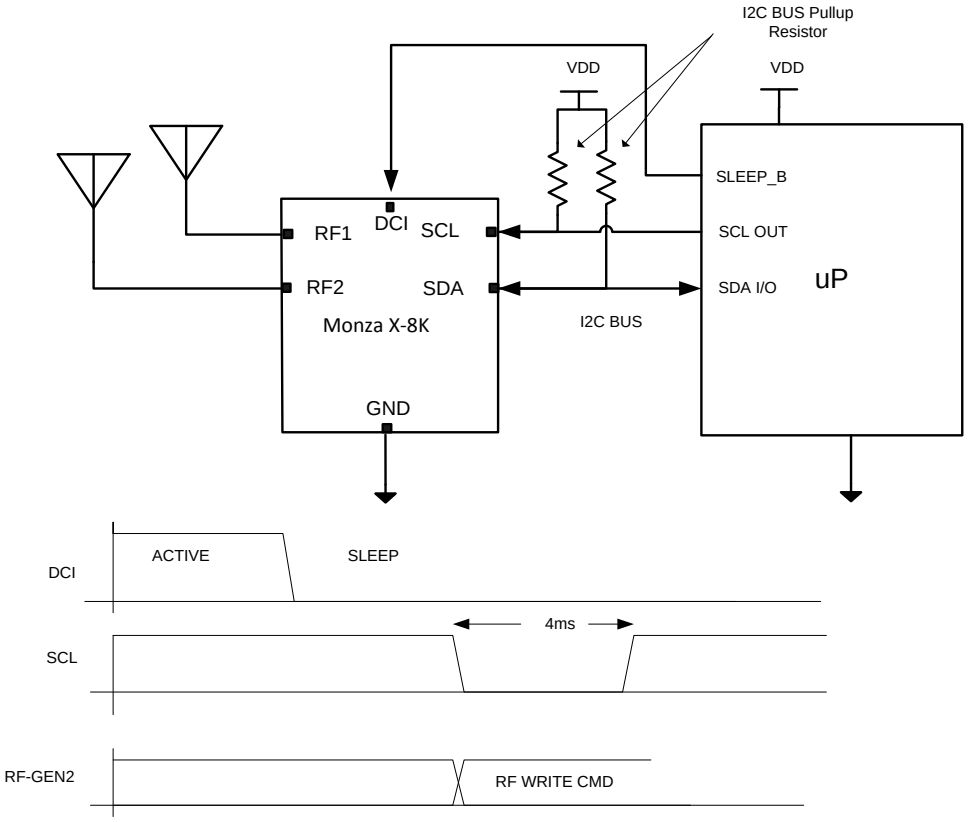


Figure 11 – Monza® X-8K Dura write wake up mode schematic and timing diagram

3 Chip Characteristics

3.1 Physical Characteristics

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
IC package	Chip package	All	XQFN 8L 2.00×2.00×0.35mm				
Pin count	Package pins	All		8		pins	2 – Port1 RF+/– 2 – Port2 RF+/– 2 – DCI/gnd 2 – I2C(SDA/SCL)

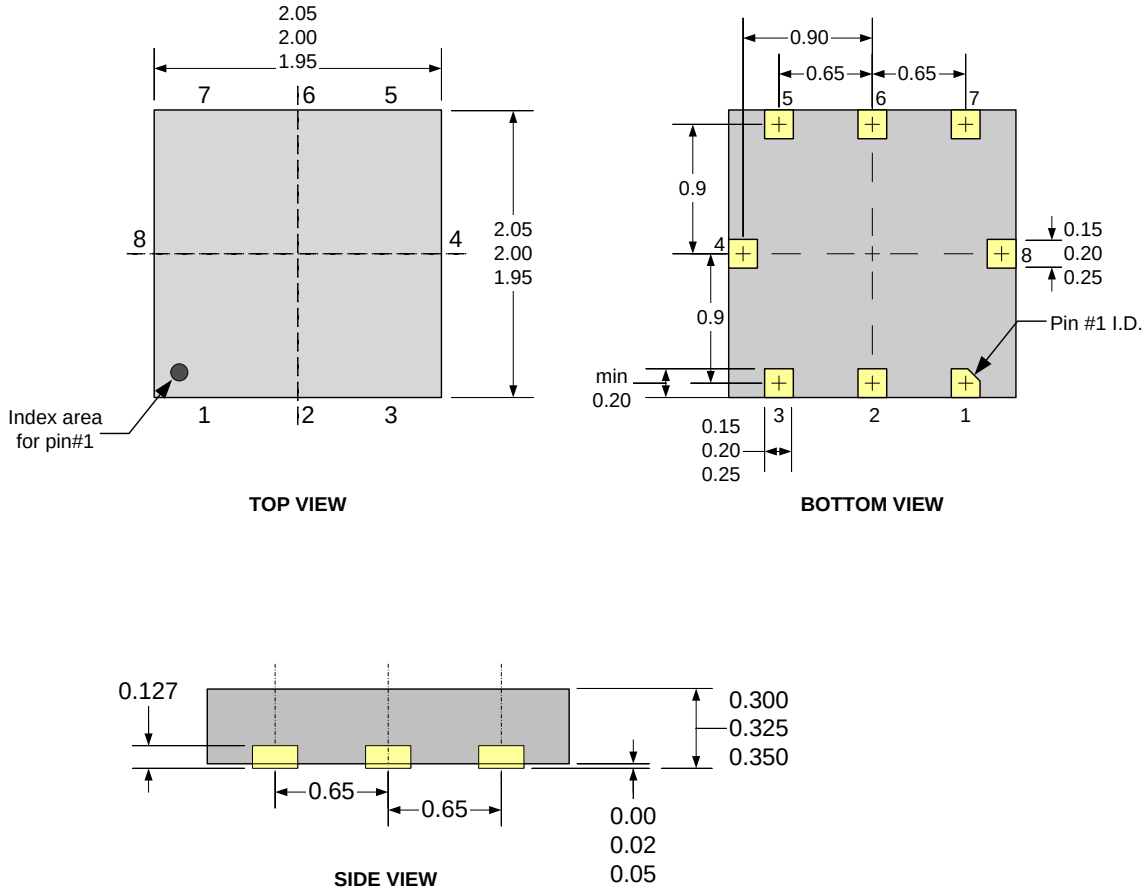


Figure 12– Packing Dimensions

3.2 Absolute Maximum Ratings

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
Absolute maximum pin voltage	Absolute maximum voltage on any chip pin	All except DCI	–0.3		4.1	V	From the I2C spec, the max DC voltage is 3.3V+20% (max operating voltage) + 0.5V for survivability
ESD		HBM	2			kV	
		CDM	500			V	
Operating Temperature	Temperature for full specified performance		-25		+85	°C	See Read/Write Sensitivity for temperature ranges in Section 3.4
Persistence Temperature	Temperature for Gen2 flag persistence		-25		+40	°C	As per the Gen2 v.1.2.0 specification for flag persistence
Storage temperature	Temperature for 10-yr NVM retention		–40		+85	°C	See Impinj's NVM usage model
Assembly survival temp	Temperature for reflow soldering / assembly				+260	°C	Peak temp of JEDEC-MO255 for lead free soldering
Moisture Sensitivity Level	Moisture/Reflow Sensitivity Classification			MSL 1			According to IPC/JEDEC's J-STD-20

3.3 Reflow Temperature Profile

3.4 Electrical Characteristics

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
RF Performance							
S_{READ}	Matched RF Input Read Sensitivity DRM, M=4	No DC Input		-17		dBm	Using DC Input, Monza X-8K Dura can be used in Battery Assisted Passive mode to increase read/write range
		With DC Input at 0°C to +85°C		-24		dBm	
		With DC Input at 0°C to -25°C		-20		dBm	
S_{WRITE}	Matched RF Input Write Sensitivity DRM, M=4	No DC Input		–12		dBm	
		With DC Input at 0°C to +85°C		-24		dBm	
		With DC Input at 0°C to -25°C		-20		dBm	
Rp	Parallel Equivalent Real Input Impedance	At Sensitivity		1600		Ohms	
Cp	Parallel Equivalent RF Input Capacitance			1		pF	

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
POWER							
V_{DCI}	DCI Input Voltage/I2C Reference		1.6		3.6	V	These DCI voltages are with a ±100mV tolerance
I_{DCW}	Current drawn by chip during write	$1.6<V_{DCI}<2.0$		100	200	µA	Nominal 80uA at 1.6V
		$2.0<V_{DCI}<3.6$		140	220		
I_{DCI}	Current drawn by chip during read or idle	$1.6<V_{DCI}<2.0$		15	30	µA	
		$2.0<V_{DCI}<3.6$		20	40		
T_{PU}	Power Up Time. Time from V_{DCI} applied until I2C accepts transactions.	V_{DCI}=1.6V			2	ms	NOTE: I2C will not interrupt a write operation. This could delay I2C access up to 20ms if RF is writing.
V_{RF_EN}	Max Vdd for which RF will always be enabled				0.25	V	Applies if the DCI_RF_EN bit is set to 0.
V_{RF_DIS}	Min Vdd for which RF will always be disabled						

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
I2C							
V_{IH}	HIGH-level input voltage	All	70%			$\%V_{DCI}$	From the section 6 of the I2Cspecification
V_{IL}	LOW-level input voltage	All			30%	$\%V_{DCI}$	
V_{HYS}	Input hysteresis	All	0.1			V	
I_{OL}	LOW-level output current	V_{OL}=0.4	3**			mA	
T_{OF}	Output Fall Time	Bus C= 40-400pf	20		250	ns	
C_I	Pin Capacitance				10	pF	Total capacitive load on the SDA/SCL pins
I_{IL}	SCL/SDA Input Leakage Current	Vin=3.7V 0V<V_{DCI}<3.7V		1	100	nA	Exceeds I2C spec of 10uA

**I_{OL} is tested with worst case minimum pull-up resistance value of 536 ohms at 2v. Applications should use as high pull-up resistance as possible consistent with the bus capacitance for the application. See the I2C specification for choosing pull-up resistor values. Values of 5K or more are typical in low power applications

3.5 Memory Characteristics

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
EPC memory	EPC NVM	In private mode only		128		bits	User writeable. This memory is hidden over RF when QT is enabled.
User memory	Total user NVM	In private mode only		8192		bits	User defined memory space. This memory is hidden over RF when QT is enabled
QT alternative EPC	Alternative EPC presented during RF singulation	In public mode only		96		bits	A user can switch the tag's RF QUERY–ACK response from EPC to alternative EPC using the QT command
Kill/Access Passwords	Password NVM	Access required		64		bits	Standard 32-bit Gen2 access and kill passwords
TID mfg#/serial#	TID ROM	In private mode only		96		bits	TID serial number is hidden over RF when QT is enabled
T_{WRITE}	Memory write time 16 or 32 bits			4.7	5	ms	

3.6 RF Functionality

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
Air protocol	Gen2 V1.2.0	All					No recommissioning; no blockerase
RF ports	Number of RF ports	All		2			Dual-differential RF ports
RF Port Disable	NVM Settable bit per port						The operation of one or both RF ports may be disabled by setting NVM bits through the I2Cport
DC Blocks RF	NVM Settable bit						Option to allow the presence of DC to disable both RF ports

3.7 I2C Characteristics

Parameter	Description	Condition	Min	Nom	Max	Units	Comments
I2C port	Number of ports	All			1		Slave I2C (SCL/SDA)
I2C functionality	Compatible with I2C-bus specification and user manual Rev. 03 – 19 June 2007	All		R/W			An external device can R/W memory
Supported I2C features	**Features:** Start condition Stop condition Acknowledge 7-bit slave address						**Slave Configuration** mandatory mandatory mandatory mandatory
I2Cwrite size	Word size for I2C write	All	16		32	bits	Writes are on word addresses and not byte addresses
I2C read size	Word size for I2C read	All		N×8		bits	May read data 8bits at a time, where N is limited by start address and bank size
I2C memory arbitration	RF/I2C port priority	All		1st			RF/I2C arbitrate for NVM access
I2C Address	I2C Device Address	All		1101XX0			
Transfer rates	I2C transfer data rates	All	0		400	kbps	I2C fast mode

3.8 NVM Usage Model

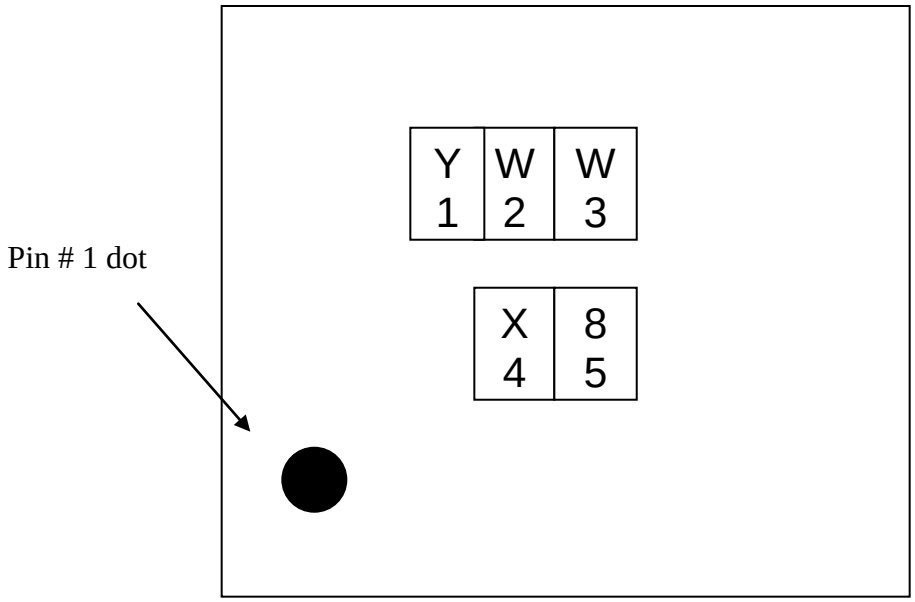
Condition			Retention (years)
Writes per row	**Total writes**	**Power-on time**	
10	100	5 yr	50
1k	10k	1 yr	10
10k	100k	2k hours	1

3.9 Environmental Compliance

Requirement	Comments
RoHS	Monza X-8K Dura is RoHS compliant. It meets the directive 2002/95/EC (RoHS). RoHS declaration letter is available upon request.
REACH	Monza X-8K Dura does not, to our current knowledge, contain substances above the legal threshold that are on the Candidate List of Substances of Very High Concern (SVHC). Our company's intention is that all products sold to our EU and EEA customers by our legal entities in Europe are compliant with REACH regulatory requirements. REACH declaration letter is available upon request.

4 Product Delivery Specifications

4.1 Marking Specification

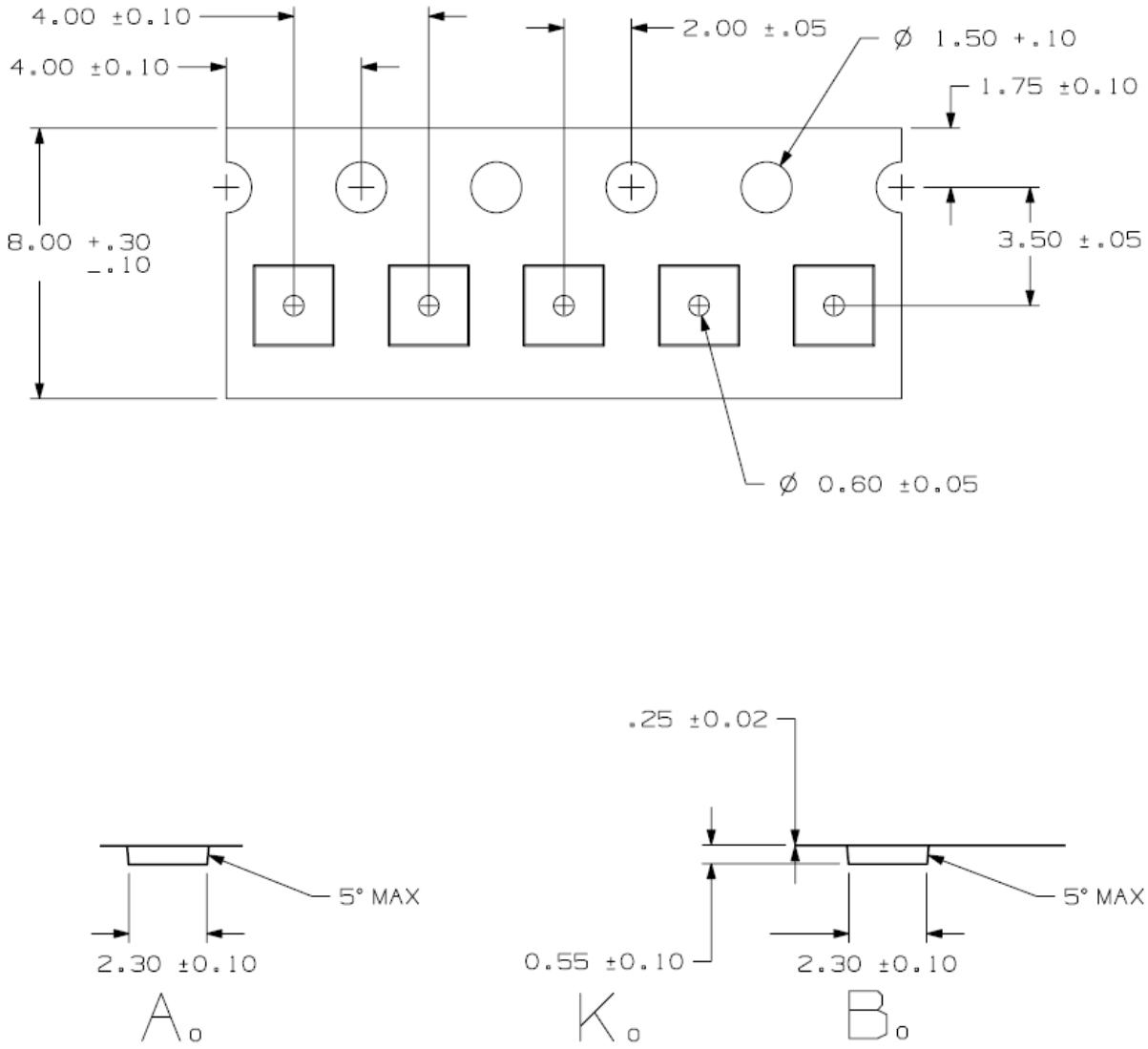


Y= Year of production (1 = 2011, 2 = 2012 …)

WW = Work Week of production

X8 = Product Code (Monza X-8K Dura)

4.2 Tape and Reel Specification



Parts per reel / Minimum order quantity: 3000

5 Footprint Compatibility with Impinj® Monza® X-2K Dura

Monza® X-8K Dura (Part Order#: IPJ-P6005-X2AT) is a higher memory capacity version of Monza® X-2K Dura (Part Order#: IPJ-P6001-Q2AT).

Monza® X-2K Dura is designed to have 2176 bits of user NVM, enabling more OTP blocks. Its package dimensions are 1.6x1.6x0.5 mm. It is designed to be a drop-in replacement for Monza X-8K Dura if the layout footprint recommended below is used. For more details about the Monza® X-2K Dura including product availability, please contact Impinj.

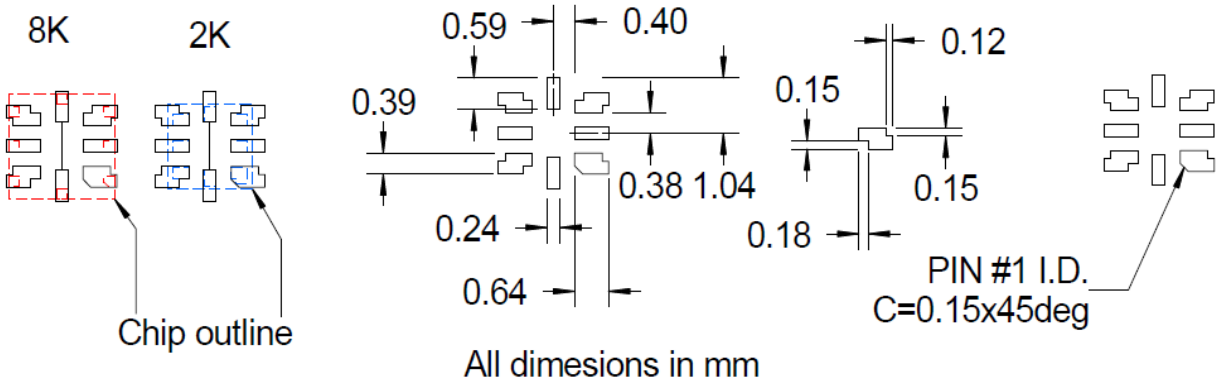


Figure 13 – Recommended common layout footprint for Monza® X-8K Dura and Monza® X-8K Dura

6 Ordering Information

Model	Part Number	User Memory	Package Size
Monza X-2K Dura	IPJ-P6001-Q2AT	2,176 bits	1.6 x 1.6 x 0.35 mm
Monza X-8K Dura	IPJ-P6005-X2AT	8,192 bits	2.0 x 2.0 x 0.35 mm

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